WEST Search History

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DATE: Friday, January 28, 2005

09/998,399

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		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L10	L6 AND ((Dual OR SINGLE) NEAR2 (In$1line OR Memory OR Module) OR 'DIMM' OR 'SIMM')	8
☐	L9	('6668196')!.PN.	2
☐	L8	('4907278')!.PN.	2
☐	L7	('20030093743')!.PN.	2
☐	L6	L5 OR L4	10
☐	L5	L2 AND TEST$3 WITH ('CRC' OR CYCLIC$4 NEAR2 (REDUNDAN$3 OR CHECK$3 OR SUM)) WITH (EXPECTED OR COMPAR$4) SAME (END) SAME (MEMORY OR 'RAM' OR 'ROM' OR ARRAY)	1
☐	L4	L2 AND TEST$3 WITH ('CRC' OR CYCLIC$4 NEAR2 (REDUNDAN$3 OR CHECK$3 OR SUM)) WITH (EXPECTED OR COMPAR$4) SAME COMPLET$3 SAME (MEMORY OR 'RAM' OR 'ROM' OR ARRAY)	9
☐	L3	L2 AND TEST$3 WITH ('CRC' OR CYCLIC$4 NEAR2 (REDUNDAN$3 OR CHECK$3 OR SUM)) WITH (EXPECTED OR COMPAR$4) SAME COMPLT$3 SAME (MEMORY OR 'RAM' OR 'ROM' OR ARRAY)	0
☐	L2	L1 AND TEST$3 WITH ('CRC' OR CYCLIC$4 NEAR2 (REDUNDAN$3 OR CHECK$3 OR SUM)) WITH (EXPECTED OR COMPAR$4)	223
☐	L1	TEST$3 SAME ('CRC' OR CYCLIC$4 NEAR2 (REDUNDAN$3 OR CHECK$3 OR SUM)) WITH (EXPECTED OR COMPAR$4)	364

END OF SEARCH HISTORY

configured to provide test case information to the test platform 112 and to receive test case results from the test platform 112. A preferred embodiment of the test platform 112 is more particularly described in copending and coassigned U.S. Patent Application Serial Number 09/998,390, entitled "Method and System for Testing Electronic Components", which is incorporated by reference herein for all purposes. For purposes of illustration and to clearly describe the present invention, however, a simplified embodiment is discussed below with reference to FIGURE 2.

FIGURE 2 is a block diagram depicting the components that preferably comprise the test platform 112 in accordance with one embodiment of the present invention. Accordingly, the test platform 112 generally comprises one or more devices under test (DUTs), such as CPUs 210, and one or more memories 212. Other components, such as a bus arbiter, I/O chipset, debug connectors, and the like, which may be necessary for the operation of the present invention, are considered well known to a person of ordinary skill in the art, and, therefore, are neither shown nor discussed in greater detail.

The CPUs 210 are configured to perform test cases supplied by the host computer 110 (FIG. 1). The memories 212, preferably Dual In-line Memory Modules (DIMMs), Single In-line Memory Modules (SIMMs), or the like, provide memory for the execution of the test cases and storage of the test case results. In a preferred embodiment, one or more of the memories 212are replaced with a Cyclic Redundancy Checker in a Multiple Instruction Shift Register (CRC-MISR) card, which is discussed in greater detail below with reference to FIGURE 3.

FIGURE 3 is a block diagram depicting the components that preferably comprise a CRC-MISR card in accordance with one embodiment of the present invention. Accordingly, reference numeral 300 generally designates a CRC-MISR card that may be substituted for one or more of the memories 212 (FIG. 2). In the preferred embodiment, the memories 212 are DIMMs, and, therefore, the CRC-MISR card 300 preferably comprises a DIMM-form factor card 310, including a standard DIMM connector 312, configured with a CRC module 314, configuration registers 318, and, optionally, memories 316.

The CRC module 314 determines a CRC value by executing a CRC algorithm on for a range of addresses as specified by the configuration registers 318 and stores the CRC value in the one or more memories 212. Preferably, the host computer 110 (FIG. 1)